

## NOISE AND SMALL-SIGNAL DISTRIBUTED MODEL OF MILLIMETER-WAVE FETs

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## ABSTRACT

This paper presents a distributed FET model for millimeter-wave frequencies and compares experimental S-parameters with distributed and lumped model. In contrast with other circuit models which take distributed effects into account, this new one allows to predict the four noise parameters up to 40 GHz. An example is given, that shows good agreement between theoretical data and S-parameters and noise figure measurements up to 26 GHz.

## INTRODUCTION

With the movement to millimeter-wave frequencies and the good performance of FETs up to 60 GHz, sophisticated circuit models are required to predict S-parameters values especially above 26 GHz where accurate measurements of chip device are difficult. Moreover, at high microwave frequencies where the device dimensions become comparable to a wavelength, the simple lumped circuit model is invalid and must be modified.

So, for a few years, several FET models have been proposed, which include propagation effects along device electrodes considered like coupled transmission lines [1-4]. Although efficient in predicting S-parameters values, these models are not well adapted to describe FET noise behavior.

In contrast, this paper presents an alternative distributed circuit model, so-called "sliced model", that permits not only to predict small signal performance but also noise parameters up to 40 GHz, with potential application to low noise broadband amplifier design.

## THE "SLICED" FET MODEL

As shown in Fig.1, the "sliced" transistor model is composed of N identical sections sliced along the actual FET gate width W. Each section (two-port Q with Zg and Zd impedances) represents a standard lumped model of a common source MESFET with gate width W/N.

According to Fig.1, we have to look for a relation connecting the vectors  $(I_{g_i}, I_{d_i})$  and  $(V_{g_i}, V_{d_i})$  which represent the currents and voltages at the FET ports.

To do this, we start with an admittance matrix description of the  $i^{th}$  section, as illustrated in Fig.2 :

$$\begin{pmatrix} I_{g_i} \\ I_{d_i} \end{pmatrix} = (Y) \begin{pmatrix} V_{g_i} \\ V_{d_i} \end{pmatrix} \quad (1)$$

along with the Kirchoff relations :

$$V_{g_i} = V_{g_{i-1}} - Z_g I_{g_{i-1}} \quad (2)$$

$$V_{d_i} = V_{d_{i-1}} - Z_d I_{d_{i-1}} \quad (3)$$

where

$$Z_g = R_g + j L_g \omega \text{ and } Z_d = R_d + j L_d \omega$$

are the gate and drain parasitic impedances respectively. Recurrent relations between gate and drain currents can be written as :

$$I_{g_{i-1}} = I_{g_0} - \sum_{k=1}^{i-1} i_{g_k} \quad (4)$$

$$I_{d_{i-1}} = I_{d_0} - \sum_{k=1}^{i-1} i_{d_k} \quad (5)$$

After straightforward algebraic manipulation of Eqns.(1) through (5), a matrix relation is obtained between voltage vectors of first and  $i^{th}$  sections :

$$\begin{pmatrix} V_{g_i} \\ V_{d_i} \end{pmatrix} = (A_i) \begin{pmatrix} V_{g_0} \\ V_{d_0} \end{pmatrix} + (B_i) \begin{pmatrix} I_{g_0} \\ I_{d_0} \end{pmatrix} \quad (6)$$

where  $(A_i)$  and  $(B_i)$  are 2x2 matrices whose elements are functions of  $Z_g$ ,  $Z_d$  and Y-parameters defined in (1). Alternative forms for (4) and (5) can be written as :

$$I_{g_0} = \sum_{k=1}^N i_{g_k} \quad (7)$$

$$I_{d_0} = \sum_{k=1}^N i_{d_k} \quad (8)$$

Substitution of Eqns.(1) and (6) into (7) and (8) for each value of i ranging from 1 to N, gives the total admittance matrix  $(Y_T)$  of the FET :

$$\begin{pmatrix} I_{g_0} \\ I_{d_0} \end{pmatrix} = (Y_T) \begin{pmatrix} V_{g_0} \\ V_{d_0} \end{pmatrix} \quad (9)$$

Using Y to S-matrix transformation, the scattering parameters of the "sliced" model is then calculated for a determined value of N, and fitted with experimental S-parameters measured up to 26 GHz. The plots for S11 and S21 (magnitude and phase) against frequency (Fig.3a,3b) all show a good agreement with experimental values and so allow realistic prediction of FET behavior up to 40 GHz.

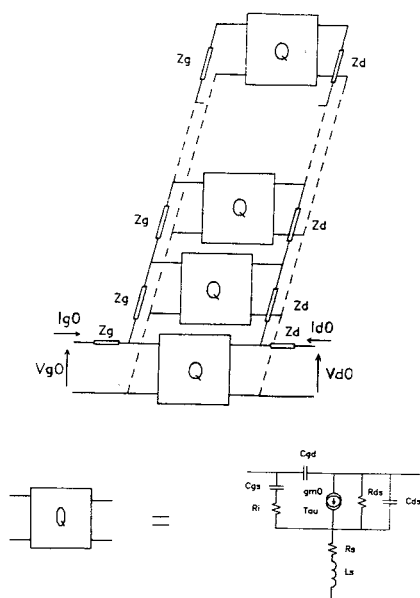


Fig. 1 : "Sliced" Transistor Model

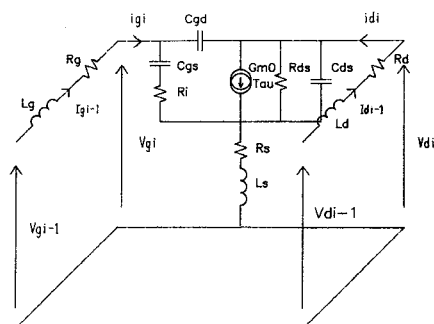


Fig. 2 : Electrical description of the  $i^{th}$  section from the "sliced" model

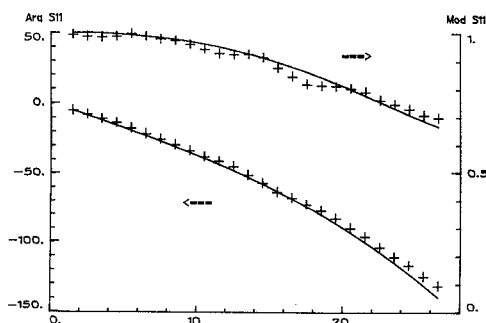


Fig. 3-a : Magnitude and phase of S11

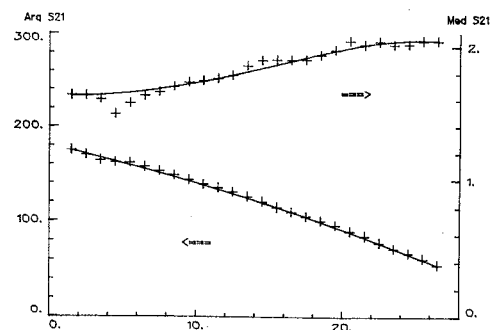


Fig. 3-b : Magnitude and phase of S21  
Fig. 3 : Optimized theoretical and experimental S-parameters from 1,5 GHz to 26,5 GHz

— "sliced" model (N=5) +++ measurements

### COMPARISON BETWEEN LUMPED, "SLICED" AND DISTRIBUTED MODEL

Taking into account propagation effects on gate and drain electrodes at millimeter waves needs the resolution of two or more coupled differential equations to obtain S-parameters [1]. In addition, noise parameters derivation from a fully-distributed model including noise sources turns out to be very complicated if not impossible.

On the other hand, the lumped model universally used in describing small-signal and noise FET behavior for X and K-bands fails out when gate width to wave-length ratio is higher than 0,1.

In contrast, this condition is always satisfied with the "sliced" model since the actual FET is considered to be electrically equivalent to N fictitious identical FETs in parallel, each of them having a gate width as small as required by a proper choice of N.

Analytical treatment is based on Kirchhoff laws applications and yields scattering and noise FET parameters with a rather tedious but straightforward manipulation (see section III).

The interest of the sliced model clearly appears in Fig.4 where the S-parameters of a FET (Thomson) have been plotted for the three models under consideration : S11, S22 on the Smith chart (Fig.4a) and S12, S21 on a polar chart (Fig.4b).

Up to about 26 GHz, the curves are all superposed, a fact which confirms the negligible propagation effects on transistor electrodes. Above 26 GHz, the lumped model S-plots spread out from the other plots which are still close to each other.

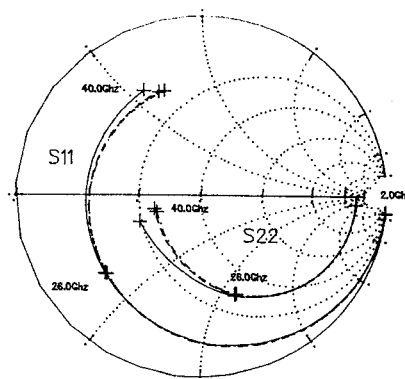


Fig. 4-a : S11 and S22 on the Smith chart

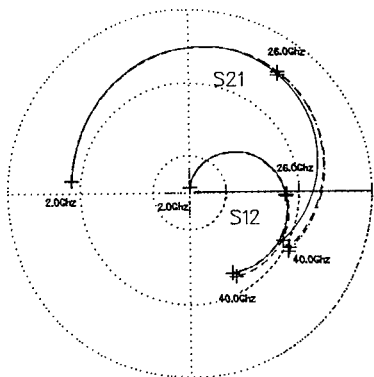


Fig. 4 : Comparison between lumped, "sliced" and distributed models from 2 to 40 GHz  
 — lumped model      --- "sliced" model (N=5)  
 -.-.- distributed model [Réf.1]

## NOISE MODELLING

The "sliced" model is extended to include the two types of noise sources shown in Fig.5 for the  $i^{\text{th}}$  section :

- intrinsic FET noise sources  $i_{ng}$ ,  $i_{nd}$  with correlation coefficient  $C$ .
- extrinsic noise sources  $i_{tg}$ ,  $i_{td}$  and  $i_{ts}$  related to FET parasitic resistances.

These are supposed to be uncorrelated from one section to the other and are characterized by their mean square values [5] [6] :

$$|\bar{i}_{ng}|^2 = 4 k T_o \Delta f \frac{\omega^2 C_{gs}^2 R}{g m_o} \quad (10)$$

$$|\overline{i_{nd}}|^2 = 4 k T_0 \Delta f g m_0 P \quad (11)$$

$$|\text{it}|^2 = 4 k T_0 \Delta f R \ell^{-1} \text{ with } \ell = g, d, s \quad (12)$$

The coefficients P, R and C, which are dependent on FET topology and bias conditions, need to be determined from noise measurements. For that, a relation between the noise factor F, the noise sources and the termination impedance  $Z_{in}$  at the FET input is derived from the method previously described in section I.

For each section of the "sliced" model (Fig.5) a matrix equation can be written as :

$$\begin{pmatrix} Vg_i \\ Vd_i \end{pmatrix} = (A_i) \begin{pmatrix} Vg_o \\ Vd_o \end{pmatrix} + (B_i) \begin{pmatrix} Ig_o \\ Id_o \end{pmatrix} + (N_i) \begin{pmatrix} i_1 \\ i_2 \end{pmatrix} \quad (13)$$

where all the V's and I's are noise voltages and currents, the index o indicating the actual FET ports. The (A<sub>o</sub>) and (B<sub>o</sub>) matrices are defined in (6). The current symbols  $i_1$  and  $i_2$  have different meanings according to the following cases:

- intrinsic gate and drain noise:  $i_1 = i_{ng}$ ,  $i_2 = i_{nd}$
- thermal noise from  $R_s$ :  $i_1 = i_2 = i_{ts}$
- thermal noise from  $R_g, R_d$ :  $i_1 = i_{tg}$ ,  $i_2 = i_{td}$
- thermal noise form termination impedance  $Z_{in}$  :  $i_1 = i_2 = 0$

The  $(N_i)$  matrix is different for each case and its elements are related to  $Z_g$ ,  $Z_d$  and  $Y$ -parameters.

Including the noise current sources in Eqns. (1) to (3), and using (13), a matrix equation between noise currents and voltages at the FET ports is obtained as :

$$\begin{pmatrix} \text{Ig}_o \\ \text{Id}_o \end{pmatrix} = (\text{Y}_T) \begin{pmatrix} \text{Vg}_o \\ \text{Vd}_o \end{pmatrix} + (\text{N}_T) \begin{pmatrix} i_1 \\ i_2 \end{pmatrix} \quad (14)$$

where  $(Y_T)$  is the total noise less FET admittance matrix and  $(N_T)$  is a noise matrix depending on the  $i_1$  and  $i_2$  currents.

Now, if the FET output is matched and its input loaded by the impedance  $Z_{in}$ , Equation (14) can be transformed into :

$$(C_T) \begin{pmatrix} I_{g_0} \\ Id_{\mathcal{O}} \end{pmatrix} = (N_T) \begin{pmatrix} i_1 \\ i_2 \end{pmatrix} \quad (15)$$

From resolution of Eqn.(15), an expression for  $I_{D0}$  is obtained for each vector  $(i_1, i_2)$ . The available power at the FET output, depending on  $|I_{D0}|^2$ , is then calculated in the four cases. The sum of these four powers divided by part of them due to the termination impedance  $Z_{in}$  gives the noise factor  $F$  :

$$F=1+\{K_1|\overline{i_{ng}}|^2+K_2|\overline{i_{nd}}|^2+2\operatorname{Re}(K_1K_2^*\overline{i_{ng}}\overline{i_{nd}}^*)+K_3|\overline{i_{tg}}|^2+K_4|\overline{i_{td}}|^2+K_5|\overline{i_{sg}}|^2\}/K_6|\overline{e_{in}}|^2 \quad (16)$$

$$\text{with } |e_{in}|^2 = 4 k T_0 \Delta f \operatorname{Re}(Z_{in}) \quad (17)$$

The coefficients  $K_j$  are depending on impedance  $Z_{in}$  and  $C_T$  and  $N_T$ -parameters. The coefficients  $P$ ,  $R$  and  $C$  are then determined by fitting the noise factor derived from the "sliced" model (Eqn.(16)) with experimental values.

For example, ten measurements of  $F$  were done for ten  $Z_{in}$  values at five frequencies ranging in the 18–26 GHz band. Results are presented in Table 1 for two bias conditions ;  $V_{ds}=3V$  and  $I_{ds}$ =either  $I_{dss}$  or  $I_{dss}/3$ . It will be noted that the  $P$ ,  $R$  and  $C$  values were obtained from averaging process over the ten measurements. Determination of these three coefficients allows to evaluate noise factor  $F$  in order to determine FET noise parameters as explained in the following section.

Bias Conditions	P	R	C
3V <sub>dss</sub>	0.32	0.09	0.83
3V <sub>dss</sub> /3	0.13	0.03	0.73

Table 1 : Optimized coefficients P,R and C for two bias conditions

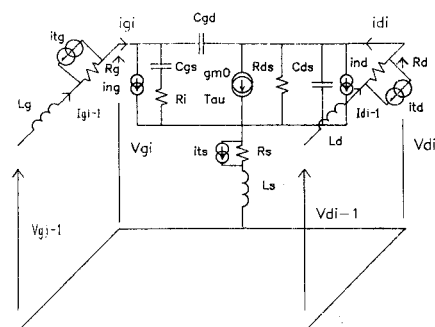


Fig. 5 : i<sup>th</sup> section of the "sliced" model with noise sources

## DETERMINATION OF FET NOISE PARAMETERS

As is well known, the FET noise behavior can be characterized by the four noise parameters  $F_o$ ,  $R_n$ ,  $R_o$ ,  $X_o$  according to the equation :

$$F = F_o + \frac{R_n}{R_{in}} \times \frac{[(R_{in} - R_o)^2 + (X_{in} - X_o)^2]}{(R_o^2 + X_o^2)} \quad (18)$$

where

$F$  noise factor

$R_n$  equivalent noise resistance

$Z_{in} = R_{in} + jX_{in}$  input termination impedance

$F_o$  minimum noise factor

$Z_o = R_o + jX_o$  optimum termination impedance that gives minimum noise factor

Determination of these noise parameters obeys

to the following steps :

1) Derivation of Eqn.(16) with respect to  $R_{in}$  and  $X_{in}$ , then cancellation of the two expressions

$\frac{\partial F}{\partial R_{in}}$  and  $\frac{\partial F}{\partial X_{in}}$  gives  $R_o$  and  $X_o$

2) Substitution  $R_o$ ,  $X_o$  for  $R_{in}$ ,  $X_{in}$  into Eqn.(16) yields the minimum noise factor  $F_o$ .

3) Computation of  $F_{50}$  from Eqn.(16) with  $Z_{in} = 50\Omega$  and identification with Eqn.(18) gives  $R_n$ .

Results for minimum noise figure  $F_o$  and equivalent noise resistance  $R_n$  are presented in Fig.6 and 7, for the two bias conditions ( $I_{dss}$  and  $I_{dss}/3$ ) and frequency ranging from 18 to 40 GHz. Experimental values of  $F_o$  and  $R_n$  have been extracted from noise figure measurements up to 26 GHz according to the method described by Mitama and al. [7].

Theoretical curves are plotted for the "sliced" model (solid line) and the lumped model (dashed line). Fig.6 shows a good agreement between theoretical and experimental values of minimum noise figure. The two straight lines curves intersect according to the decreasing of cut-off frequency with smaller drain current.

Moreover, the spreading of the two types of curves around 26 GHz confirms the limit of lumped model validity previously shown in section II.

In Fig.7, the fit between experimental and "sliced" model derived  $R_n$  values is reasonably good, but the evolution of  $R_n$  against frequency is difficult to explain.

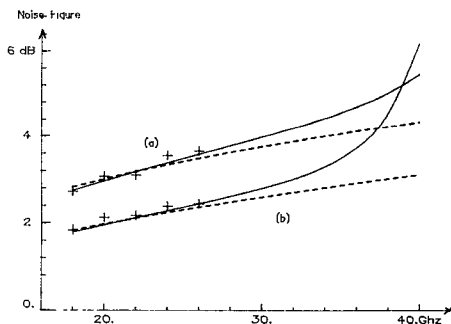


Fig. 6 : Minimum noise figure against frequency from 18 to 40 GHz

+++ experimental value — "sliced" model (N=5)

--- lumped model

(a)  $V_{ds}=3V$ ,  $I_{ds}=I_{dss}$

(b)  $V_{ds}=3V$ ,  $I_{ds}=I_{dss}/3$

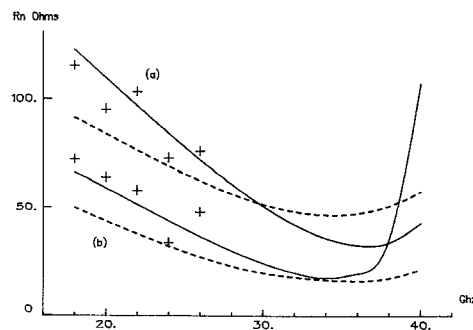


Fig.7: Equivalent noise resistance against frequency from 18 to 40 GHz

+++ experimental values — "sliced" model (N=5)

--- lumped model

(a)  $V_{ds}=3V$ ,  $I_{ds}=I_{dss}$  (b)  $V_{ds}=3V$ ,  $I_{ds}=I_{dss}/3$

## CONCLUSION

A new distributed FET model, so-called "sliced" FET model, is presented in this paper, that allows to predict S-parameters up to millimeter-wave frequencies from microwave measurements. In addition, the four noise parameters can be determined up to 40 GHz from noise figure measurements. At our knowledge, it is the first time that a FET device is so fully characterized with a distributed circuit model, that exhibits good agreement with experimental data up to 26 GHz.

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